IN THE SPECIFICATION:

Add the following new paragraph after the title ending on line 3 of page 1:

This is a Divisional Application of U.S. Patent Application Serial No. 10/115,208, filed on April 4, 2002, which is hereby incorporated by reference.

Heading beginning at page 1, line 16 has been amended as follows:

2. Description of the [[Prior]] Related Art

Paragraph beginning at page 1, line 17 has been amended as follows:

[[The]] A high-dielectric layer such as [[the]] a BST ($(Ba,Sr)TiO_3$) layer, [[the]] an ST ($SrTiO_x$) layer, [[the]] a Ta_2O_5 layer, etc. and [[the]] a ferroelectric layer such as [[the]] a PZT ($PbZr_xTi_{1-x}O_3$) layer, etc., are widely used as [[the]] a capacitor dielectric layer in a DRAM (Dynamic Random Access Memory), a FeRAM (Ferroelectric Random Access Memory), etc., by employing positively [[the]] a high dielectric constant and [[the]] an inverted polarization characteristic.

Paragraph beginning at page 1, line 25 has been amended as follows:

Also, in [[the]] a ferroelectric capacitor of FeRAM, [[the]] a planar-type capacitor having [[the]] a structure in which [[the]] a connection between the lower electrode of the capacitor and the impurity diffusion region of the transistor is extracted from the upper side of the lower

electrode is practically used. In this case, [[the]] a stacked-type capacitor having [[the]] a structure in which the lower electrode is connected to the impurity diffusion region via the conductive plug formed immediately under the lower electrode is required in the future to reduce [[the]] cell area.

Paragraph beginning at page 2, line 9 has been amended as follows:

If the high-dielectric oxide layer or the ferroelectric oxide layer is used as the capacitor dielectric layer, platinum (Pt) is widely used as the electrode material. This is because the conductivity of the platinum is high, [[the]] platinum can withstand the high-temperature process in the course of formation of the dielectric layer, [[the]] and platinum can control the orientation direction of the capacitor dielectric layer formed thereon, etc.

Paragraph beginning at page 2, line 18 has been amended as follows:

On the contrary, [[the]] platinum has [[the]] high oxygen permeability. Therefore, if the lower electrode made of [[the]] platinum is formed on the plug in the stacked-type capacitor, [[the]] oxygen can transmit through the lower electrode in the annealing process in the course of the formation of the capacitor dielectric layer to oxidize the plug. As a result, for example, if the plug is formed of tungsten, [[the]] an insulating tungsten oxide layer is formed between the plug and the lower electrode and, thus, [[the]] contact between the plug and the lower electrode is lost.

Paragraph beginning at page 3, line 2 has been amended as follows:

Therefore, in the stacked-type capacitor, the stacked structure such as the Pt/Ir structure in which the Ir layer and the Pt layer are formed sequentially from the bottom, the Pt/IrO_2 structure in which the IrO_2 layer and the Pt layer are formed sequentially from the bottom, the $Pt/IrO_2/Ir$ structure in which the Ir layer, the IrO_2 layer, and the Pt layer are formed sequentially from the bottom, or the like, is employed as the lower electrode structure.

Paragraph beginning at page 3, line 11 has been amended as follows:

The iridium (Ir) layer and the iridium oxide (IrO_2) layer has [[the]] a very small oxygen permeability and acts as [[the]] an oxygen barrier in the annealing process. Therefore, if this layer is formed as the underlying layer of the platinum layer serving as the lower electrode of the stacked-type capacitor, [[the]] oxidation of the plug under the lower electrode can be prevented in the course of the formation of the capacitor dielectric layer.

Paragraph beginning at page 3, line 27 has been amended as follows:

However, in the case that the PZT layer deposited by [[the]] a sputtering method is applied as the capacitor dielectric layer, it is found that, if the lower electrode structure containing the iridium-based oxygen barrier layer (Ir layer, IrO_2 layer) is employed, [[the]] an increase in the leakage current of the capacitor is brought about.

Paragraph beginning at page 4, line 7 has been amended as follows:

If the PZT layer is deposited on the lower electrode by [[the]] sputtering, the as-deposited PZT layer is in [[the]] an amorphous state and [[the]] a high-temperature annealing process is needed to crystallize the PZT layer.

Paragraph beginning at page 7, line 19 has been amended as follows:

Therefore, the electric connection between the conductive plug and the lower electrode can be improved, and also [[the]] sufficient crystallization of the capacitor dielectric layer can be achieved while preventing the diffusion of the first metal into the dielectric layer after the dielectric layer is formed on the lower electrode. As a result, [[the]] high performance capacitor having the desired electric characteristics can be manufactured.

Paragraph beginning at page 12, line 26 has been amended as follows:

In this manner, the main feature of the capacitor according to the first embodiment resides in that the lower electrode 30 is formed of the stacked layer consisting of the iridium layer 18, the iridium oxide layer 20, the platinum oxide layer 22, and the platinum layer 24. The reason ~~for the structure that the lower electrode 30 is constructed by~~ such a stacked structure in the capacitor according to the first embodiment will be explained hereunder.

Paragraph beginning at page 13, line 8 has been amended as follows:

The iridium layer 18 and the iridium oxide layer 20 are layers serving as [[the]] an oxygen barrier. As described above, the platinum layer 24 is the layer having the high oxygen permeability. Thus, unless the oxygen barrier layer is provided under the platinum layer 24, the oxygen is diffused toward the plug 16 in the course of the layer formation of the capacitor dielectric layer 32 or in the course of the crystallization thereof and thus at least an upper surface of the plug 16 is oxidized. If the iridium layer 18 and the iridium oxide layer 20, both having [[the]] low oxygen permeability, are provided between the plug 16 and the platinum layer 24, the plug 16 is never oxidized in the course of the layer formation of the capacitor dielectric layer 32 or in the course of the crystallization thereof. Thus, the contact characteristic between the plug 16 and the lower electrode 30 can be held satisfactorily.

Paragraph beginning at page 13, line 25 has been amended as follows:

The reason for forming the iridium oxide layer 20 in addition to the iridium layer 18 is to provide [[the]] sufficient orientation to the platinum layer 24 formed thereon. The platinum layer 24 can be oriented only by the iridium layer 18, but the orientation of the iridium layer 18 is reflected on the platinum layer 24. In order ~~to give~~ provide a much more the sufficient orientation to the platinum layer 24 ~~much more~~, it is desired that the iridium oxide layer 20 should be formed in addition to the iridium layer 18.

Paragraph beginning at page 14, line 7 has been amended as follows:

The platinum oxide layer 22 is the iridium diffusion preventing layer that prevents the diffusion of the iridium from the oxygen barrier layer (the iridium layer 18 and the iridium oxide layer 20) to the capacitor dielectric layer 32. As described above, if the PZT layer deposited by the sputter method is applied as the capacitor dielectric layer 32, the iridium is diffused into the PZT layer from the iridium-based oxygen barrier layer via the Pt layer and thus the leakage current of the capacitor is increased. Therefore, if the platinum oxide layer 22 that has the high iridium diffusion preventing capability is formed on the oxygen barrier layer, the iridium can be prevented from being diffused into the PZT layer in the course of the annealing process as the post process. As a result, the crystallization of the capacitor dielectric layer 32 can be achieved sufficiently and, thus, the capacitor dielectric layer 32 having the desired dielectric constant can be formed.

Paragraph beginning at page 14, line 25 has been amended as follows:

FIG.2 is a graph showing results of the iridium distribution in the capacitor in the depth direction, which [[are]] <u>is</u> measured by the secondary ion mass spectrometry method. In FIG.2, a dotted line indicates the case where the electrode structure of the capacitor according to the first embodiment is employed, and a solid line indicates the case where the $Pt/IrO_x/Ir$ electrode structure in the prior art is employed. As shown in FIG.2, the iridium is seldom watched in the PZT layer in the capacitor according to the first embodiment indicated by the dotted line, but the

iridium is watched at the high concentration in the capacitor having the $Pt/IrO_x/Ir$ electrode structure indicated by the solid line. It can be understood from FIG.2 that the platinum oxide layer 22 that is provided between the platinum layer 24 and the iridium oxide layer 20 of the lower electrode 30 has the iridium diffusion preventing action.

Paragraph beginning at page 15, line 15 has been amended as follows:

In this case, the mechanism for preventing the diffusion of the iridium by the platinum oxide layer 22 is not apparent. [[But]] However, it may be considered that the oxygen contained in the platinum oxide layer 22 has [[the]] an important role to prevent the diffusion of the iridium.

Paragraph beginning at page 15, line 20 has been amended as follows:

The platinum layer 24 is the layer that is provided mainly to control the orientation of the crystal of the capacitor dielectric layer 32. The platinum layer 24 has [[the]] a high conductivity and is effective for the reduction in the resistance of the lower electrode 30. Also, ~~there is the merit such that~~ the platinum layer 24 has [[the]] a high melting point and can withstand the high-temperature process in the course of the formation of the capacitor dielectric layer.

Paragraph beginning at page 16, line 2 has been amended as follows:

If the capacitor is constructed in this manner, the iridium layer 18 functions as the oxygen barrier and the platinum oxide layer 22 functions as the diffusion barrier of the iridium. For this reason, the entering of the oxygen in the course of the formation of the capacitor dielectric layer 32 and the diffusion of the iridium into the capacitor dielectric layer 32 can be prevented. Therefore, [[the]] a capacitor dielectric layer 32 having the desired dielectric constant can be formed, while maintaining the contact characteristic between the plug 16 and the lower electrode 30.

Paragraph beginning at page 16, line 13 has been amended as follows:

The characteristics of the capacitor ~~due to difference~~ resulting from differences in the structures in the first embodiment and the prior art are shown in Table 1. By way of comparison, the characteristic of the capacitor having the lower electrode that has the $Pt/IrO_x/Ir$ structure, in which the iridium diffusion preventing layer is not provided, and the characteristic of the capacitor having the lower electrode that has the Pt/Ti structure, which is widely employed in the planar-type capacitor, are also shown in Table 1. In this case, the residual electric charge amount is measured at 3 V and the leakage current is measured at 6 V.

Paragraph beginning at page 17, line 26 has been amended as follows:

First, the steps required until the structure shown in FIG.3A is formed will be explained hereunder.

Paragraph beginning at page 18, line 1 has been amended as follows:

The interlayer insulating layer 12 made of the silicon oxide layer is formed by depositing the silicon oxide layer of 700 nm thickness, for example, on the silicon substrate 10 by [[the]] a CVD method, for example.

Paragraph beginning at page 18, line 5 has been amended as follows:

Then, the contact hole that reaches the silicon substrate 10 is formed in the interlayer insulating layer 12 by [[the]] lithography and [[the]] dry etching.

Paragraph beginning at page 18, line 8 has been amended as follows:

Then, a titanium (Ti) layer of 20 nm thickness, a titanium nitride (TiN) layer of 10 nm thickness, and a tungsten (W) layer of 300 nm thickness, for example, are deposited on the overall surface by [[the]] a CVD method, for example.

Paragraph beginning at page 18, line 13 has been amended as follows:

Then, [[the]] a plug 16 that consists of the stacked structure of the W/TiN/Ti structure and is buried in the contact hole 14 is formed by polishing flat the tungsten layer, the titanium nitride layer, and the titanium layer by virtue of the CMP (Chemical Mechanical Polishing) method, for example, until a surface of the interlayer insulating layer 12 is exposed (FIG.3A).

Paragraph beginning at page 18, line 22 has been amended as follows:

Next, steps required until the structure shown in FIG.3B is formed will be explained.

The iridium layer 18 of 200 nm thickness, for example, is formed on the overall surface of the interlayer insulating layer 12 and the plug 16 by [[the]] a sputter method, for example. For instance, the iridium layer 18 of 200 nm thickness is formed by growing the layer for 144 seconds at [[the]] a substrate temperature of 200 °C, the power of 1 kW, and [[the]] an argon (Ar) gas flow rate of 100 sccm.

Paragraph beginning at page 19, line 3 has been amended as follows:

Then, [[the]] an iridium oxide layer 20 of 30 nm thickness, for example, is formed on the iridium layer 18 by the sputter method, for example. For instance, [[the]] an iridium oxide layer 20 of 30 nm thickness is formed by growing the layer for 11 seconds at [[the]] a substrate temperature of 20 °C, the power of 1 kW, [[the]] an argon gas flow rate of 25 sccm, and [[the]] an oxygen gas flow rate of 25 sccm.

Paragraph beginning at page 19, line 10 has been amended as follows:

Then, [[the]] a platinum oxide layer 22 of 23 nm thickness, for example, is formed on the iridium oxide layer 20 by the sputter method, for example. For instance, the platinum oxide layer 22 of 23 nm thickness is formed by growing the layer for 27 seconds at [[the]] a substrate temperature of 350 °C, [[the]] a power of 1 kW, [[the]] an argon gas flow rate of 36 sccm, and [[the]] an oxygen gas flow rate of 144 sccm.

Paragraph beginning at page 19, line 18 has been amended as follows:

As shown in FIG.4, when the substrate temperature in forming the platinum oxide layer 22 is ~~lower~~ less than 200 °C or ~~higher~~ greater than 400 °C, the reduction in the residual electric charge amount appears. Also, as shown in FIG.5, the substrate temperature in forming the platinum oxide layer 22 is ~~lower~~ less than 200 °C or ~~higher~~ greater than 400 °C, the leakage current is increased. Also, the oxygen is dissociated during the layer formation of the platinum oxide layer 22 at [[the]] a substrate temperature of more than 400 °C, so that the platinum layer is formed. Accordingly, it is desired that the substrate temperature in forming the platinum oxide layer 22 should be set ~~over~~ to be greater than 200 °C and ~~below~~ less than 400 °C. Also, the residual electric charge amount has the larger value if the layer forming temperature becomes higher within the above temperature range. Therefore, it is desired that the substrate temperature in forming the platinum oxide layer 22 should be set to the higher temperature within the above temperature range, e.g., the temperature of about 350 °C.

Paragraph beginning at page 20, line 10 has been amended as follows:

In addition, the layer thickness of the platinum oxide layer 22 is set to 23 nm in the above layer forming conditions, but the layer thickness of more than 15 nm may be appropriately selected. The adhesiveness of the platinum oxide layer 22 is not sufficient if the layer thickness is ~~thinner~~ less than 15 nm, while the subsequent workability is degraded if the layer thickness is too ~~thick~~ great. As a result, it is desired that the layer thickness of the platinum oxide layer 22 should be appropriately selected in response to the structure of the applied system and process to exceed [[the]] a layer thickness of 15 nm.

Paragraph beginning at page 20, line 22 has been amended as follows:

Also, in the above layer forming conditions, the gas flow rate ratio in forming the platinum oxide layer 22 is set as $Ar:O_2=1:4$. As shown in FIG.6, if the gas flow rate ratio is changed in the range of $Ar:O_2=7:2$ to 1:9 (oxygen concentration 40 to 90 %), the residual electric charge amount in the formed capacitor is seldom changed. In other words, it may be considered that the gas flow rate ratio in forming the platinum oxide layer 22 does not exert a [[bad]] negative influence upon the residual electric charge amount. According to this, the gas flow rate ratio in forming the platinum oxide layer 22 may be set to any value, and preferably the oxygen concentration should be set to 40 to 80 %.

Paragraph beginning at page 21, line 8 has been amended as follows:

Then, [[the]] a platinum layer 24 of 100 nm thickness, for example, is formed on the platinum oxide layer 22 by the sputter method, for example. For instance, the platinum layer 24 of 100 nm thickness is formed by growing the layer for 54 seconds at [[the]] a substrate temperature of 13 °C, [[the]] a power of 1 kW, and [[the]] an argon gas flow rate of 100 sccm.

Paragraph beginning at page 21, line 15 has been amended as follows:

In this case, the substrate temperature in forming the platinum layer 24 is set ~~below~~ to be less than 400 °C. This is because the oxygen is dissociated from the underlying platinum oxide layer 22 if the layer is formed at the temperature of [[more]] greater than 400 °C and, thus, the iridium diffusion preventing action is degraded.

Paragraph beginning at page 21, line 21 has been amended as follows:

Then, [[the]] a rapid thermal annealing process is carried out at 600 to 750 °C in [[the]] an argon atmosphere to crystallize the platinum layer 24. [[Since]] Because the platinum layer 24 has [[the]] a predetermined orientation by this annealing process, it is possible to control the orientation of the PZT layer to be formed later.

Paragraph beginning at page 22, line 3 has been amended as follows:

Then, the PZT layer 26 is crystallized by executing the rapid thermal annealing process at 750 °C in the oxygen atmosphere. At this time, the PZT layer 26 is subjected to the orientation of the underlying platinum layer 24 and then oriented in (111). Also, [[since]] because the platinum oxide layer 22 that functions as the iridium diffusion barrier layer is formed between the PZT layer 26 and the iridium oxide layer 20, the iridium is ~~in no ways~~ not diffused into the PZT layer 26 even if such a high-temperature process is carried out.

Paragraph beginning at page 23, line 7 has been amended as follows:

As described above, according the first embodiment, the lower electrode 30 consisting of the platinum layer 24/the platinum oxide layer 22/the iridium oxide layer 20/the iridium layer 18 is formed. Thus, the diffusion of the oxygen in the course of the layer formation of the capacitor dielectric layer 32 can be prevented by the iridium oxide layer 20 and the iridium layer 18, and also the diffusion of the iridium from the oxygen diffusion barrier layer to the capacitor dielectric layer 32 can be prevented by the platinum oxide layer 22. Therefore, even if the capacitor dielectric layer 32 is formed by the sputtering, the sufficient crystallization of the capacitor dielectric layer can be achieved while preventing the diffusion of the iridium. As a result, [[the]] a high-performance ferroelectric capacitor having the desired electric characteristics can be manufactured.

Paragraph beginning at page 23, line 23 has been amended as follows:

In the above first embodiment, the lower electrode 30 is formed of the stacked layer that consists of the iridium layer 18, the iridium oxide layer 20, the platinum oxide layer 22, and the platinum layer 24. Either the iridium layer 18 or the iridium oxide layer 20 may be employed as the layer that is used as the oxygen barrier. For example, as shown in FIG.7, the lower electrode 30 may be formed of [[the]] a stacked layer that consists of [[the]] an iridium layer 18, [[the]] a platinum oxide layer 22, and [[the]] an platinum layer 24.